SRAM Design with OpenRAM in SkyWater 130nm

Jesse Cirimelli-Low, Muhammad Hadir Khan, Samuel Crow,
Amogh Lonkar, Bugra Onal, Andrew D. Zonenberg, **Matthew R. Guthaus**

University of California Santa Cruz, USA

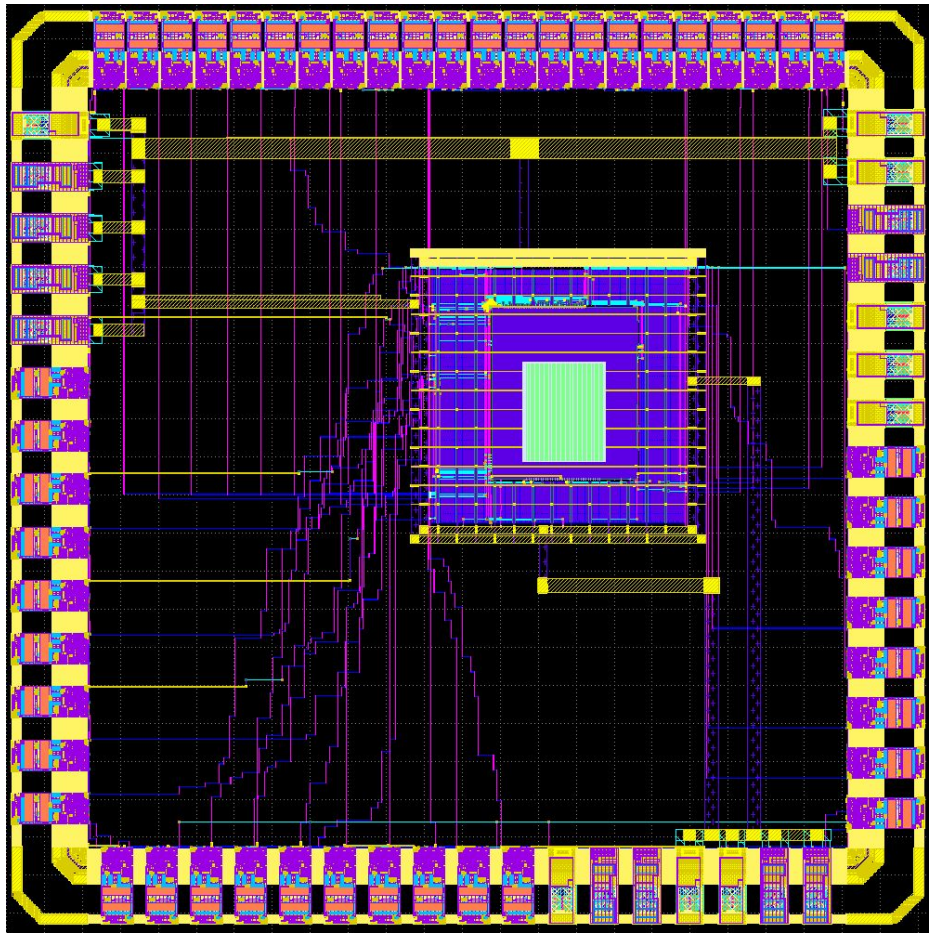
https://github.com/VLSIDA/OpenRAM

TLDR: OpenRAM

- Implemented in Python 3.5+
- Licensed with 3-clause BSD
- Provides reference circuit and physical implementations
- Provides a timing/power characterization methodology and functional verification
- Generates GDSII layout data, SPICE netlist, Verilog model, DRC/LVS verification reports and P&R macro view.
- Wrappers for both open-source and commercial tools

OpenRAM Test-Chip One (OR1)

- 32-bit
- 1kb
- 1RW1R dual port design
- Similar to 2kb dual port macro on the Caravel management core
- Developed with closed source DRC/LVS tooling



OR1 test-chip layout with 1kb dual port SRAM

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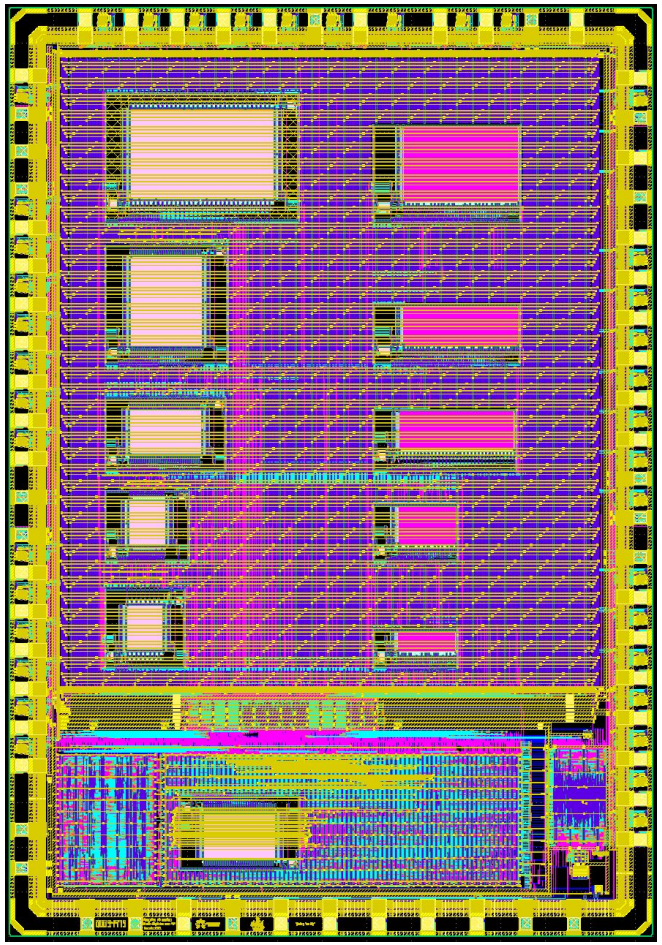
Multi-Project Wafer 2 Test Chip (MPW2)

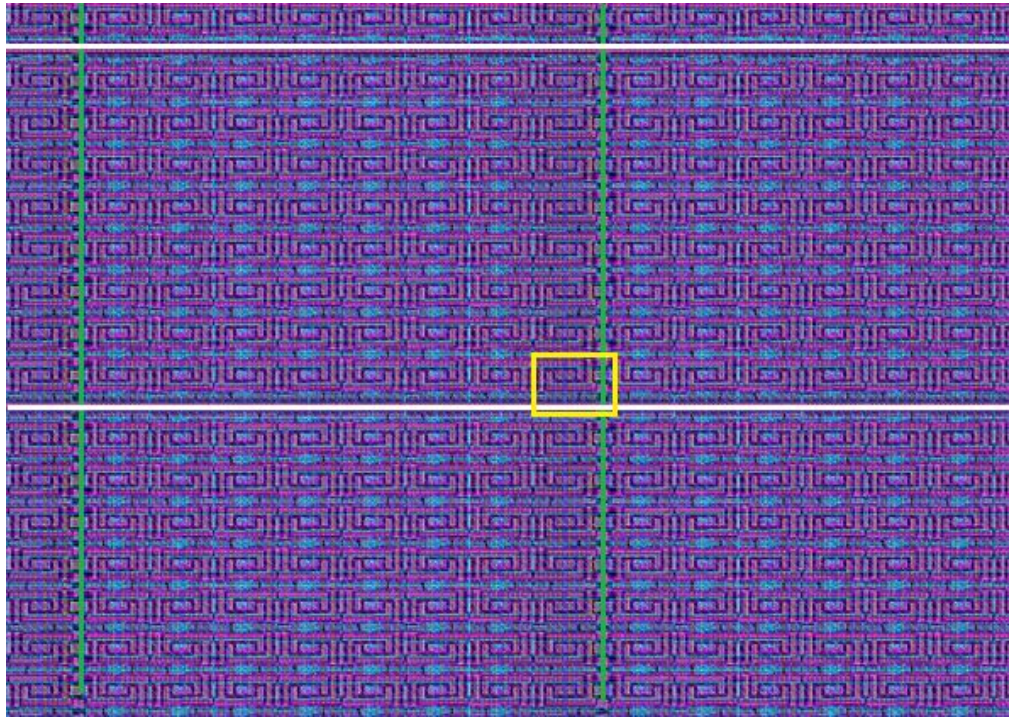


MPW2 Layout with 10 OpenRAM SRAMs and Caravel management core

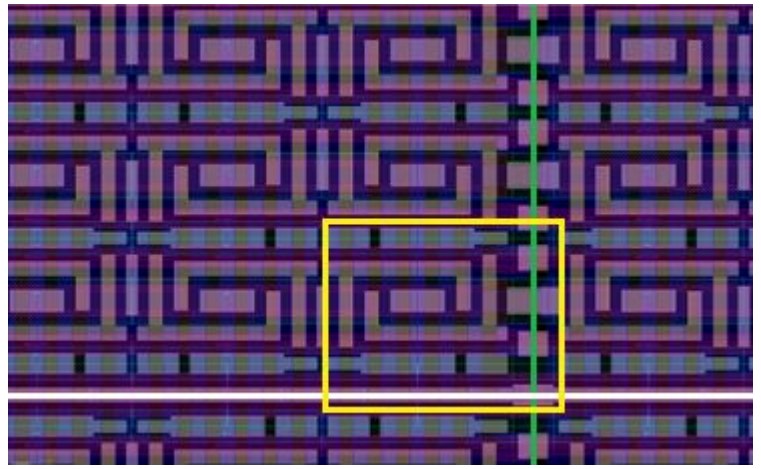
- 5 dual port + 5 single port macros
- 1-8kb 32 bit 1RW1R macros
- 1-8kb 32/64 bit 1RW macros
- Developed with entirely with open-source tools!

OpenRAM

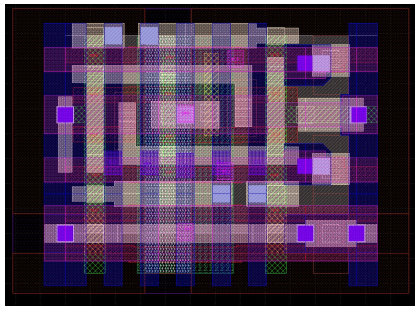
Generating Bitcells – Dual Port



Foundry dual port macro with tap cells (white), strap cells (green) and final OpenRAM bitcell (yellow)



Expanded view of foundry macro



Final OpenRAM cell

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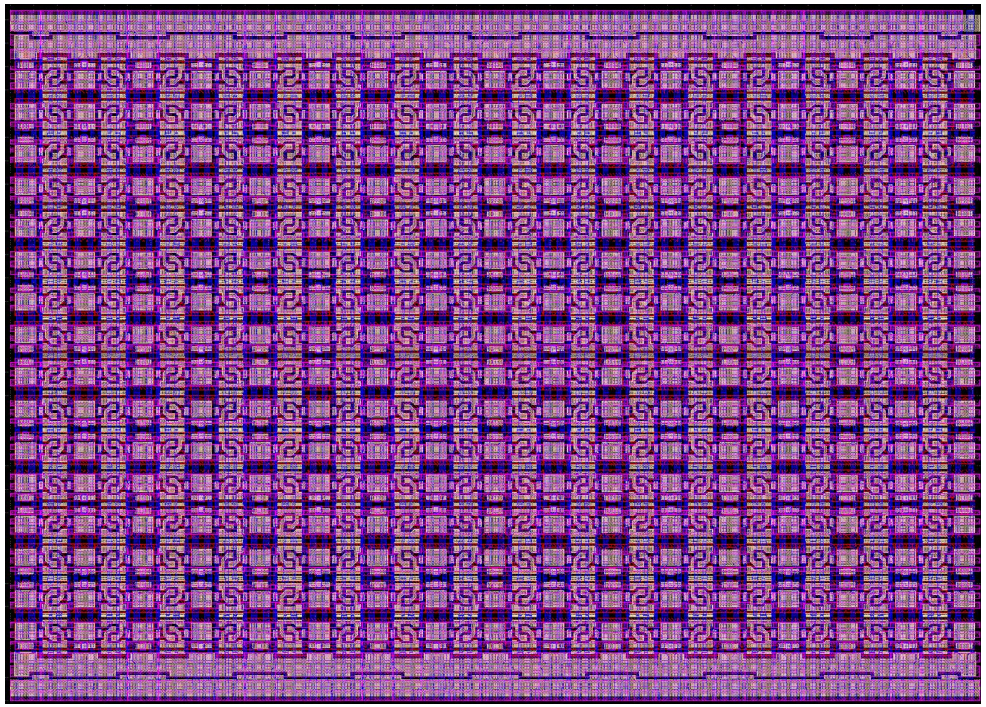
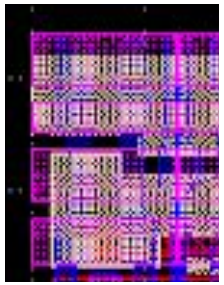
Generating Bitcells – Single Port



Foundry single port memory features cells which break user DRC users, and sensitive OPC layers



Corner, colend, and rowend cells

Bitcells

Strap cells

Extract foundry cells and reconstruct the array with OpenRAM

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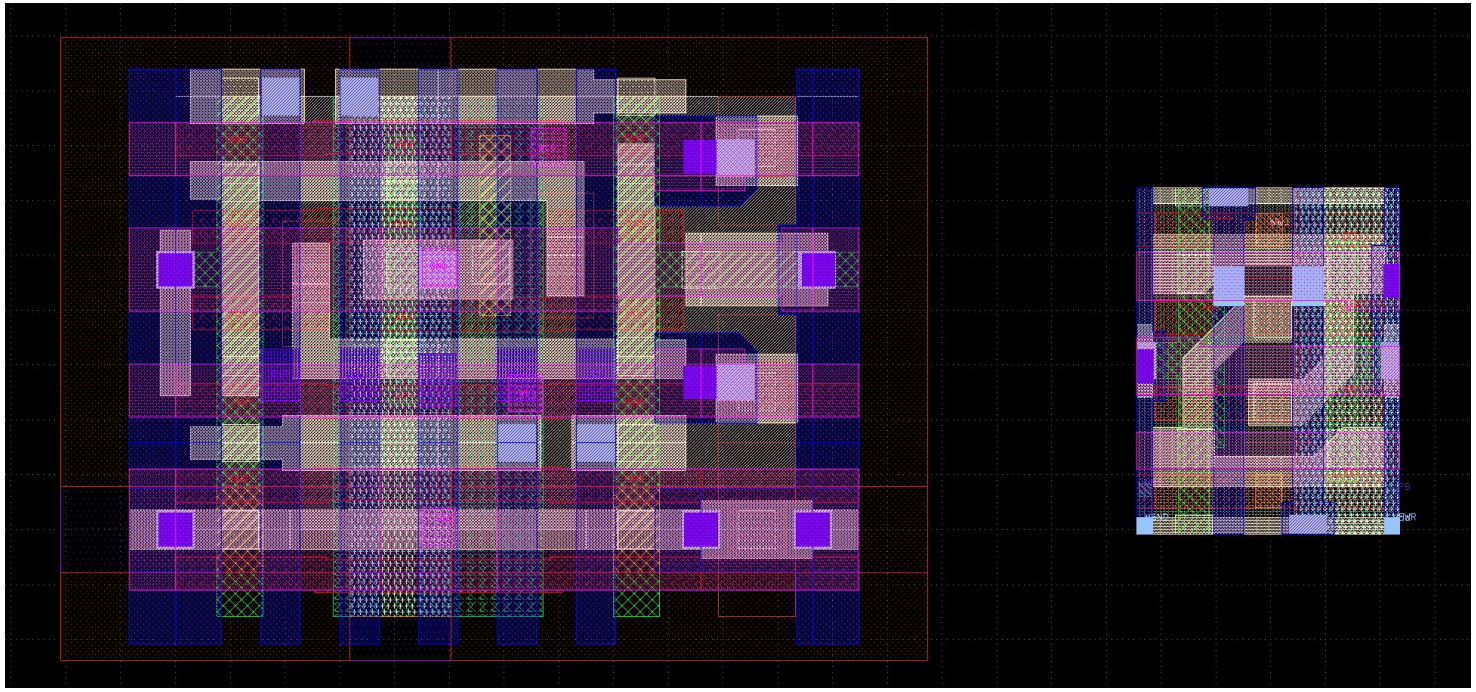
Generating Bitcells

8T cell area:
3.792µm^2

Dual port cell area:
6.162µm^2



Single port cell area:
1.896µm^2

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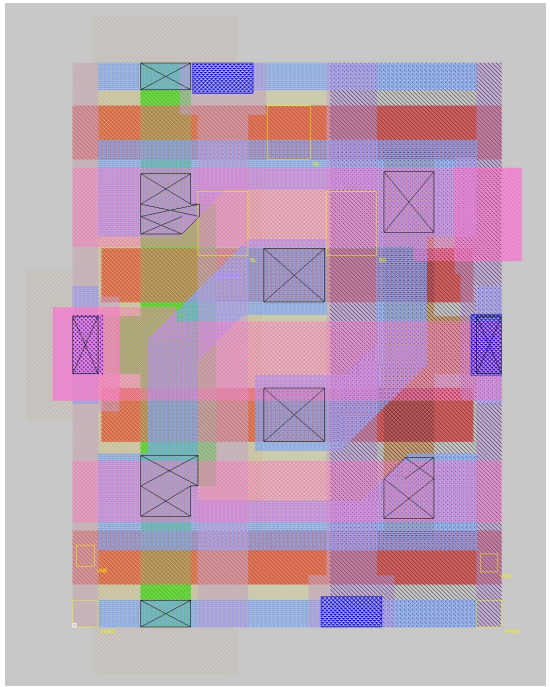
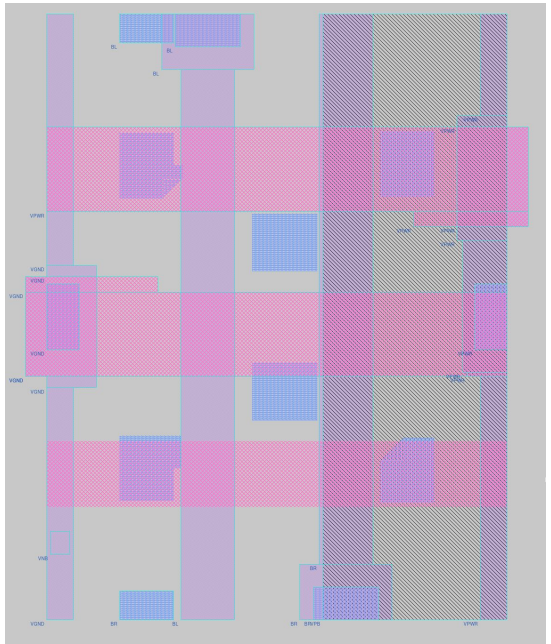
DRC With Single Port Foundry Cells

- Problem: Foundry single port SRAM cells break user DRC rules
- Solution: Use abstracted views of arrays during DRC checks



6T SRAM cell original view



6T SRAM cell LEF view

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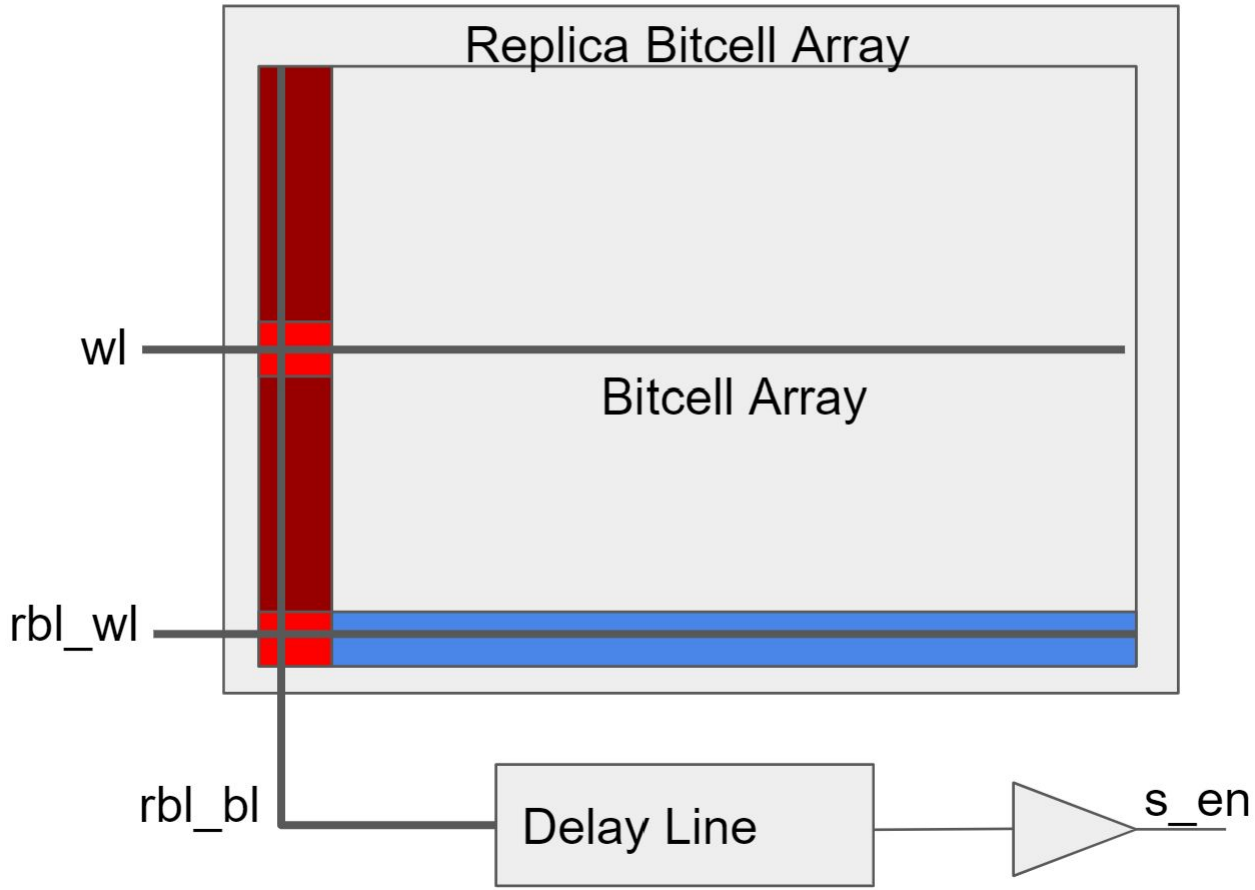
Replica Column Sensing

- Control sense amplifier timing
- Models word line and delay and bit line access time
- Tracks voltage, temp, and process variation
- **Requires additional replica cells (red) and dummy cells (blue)**



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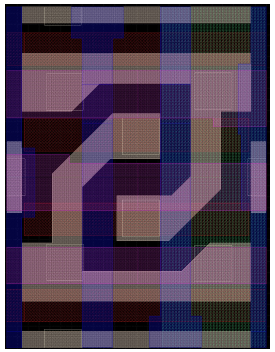
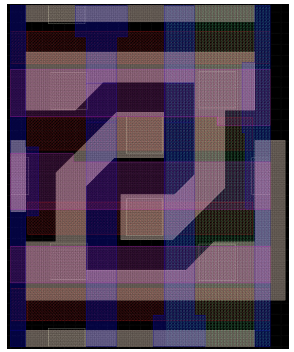
Replica Column Cells

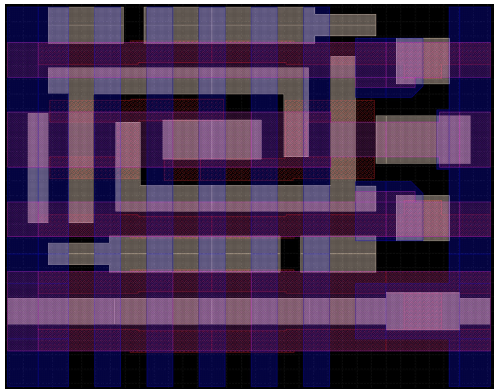
- Replica cells always store a “0”
- Additional LI shape connects the “Q” node to ground



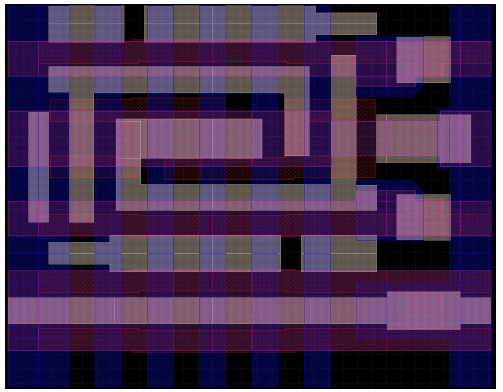
Single port array bitcell



Single port replica column bitcell



Dual port array bitcell



Dual port replica column bitcell

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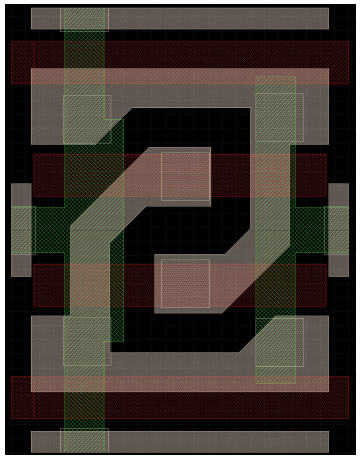
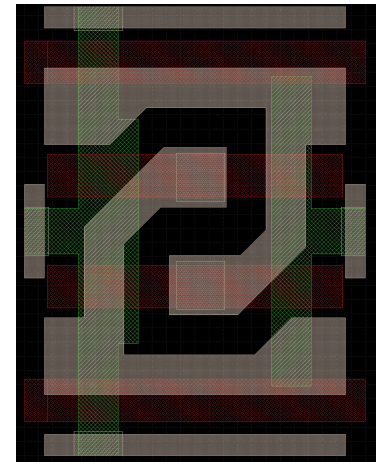
Dummy Bitcells

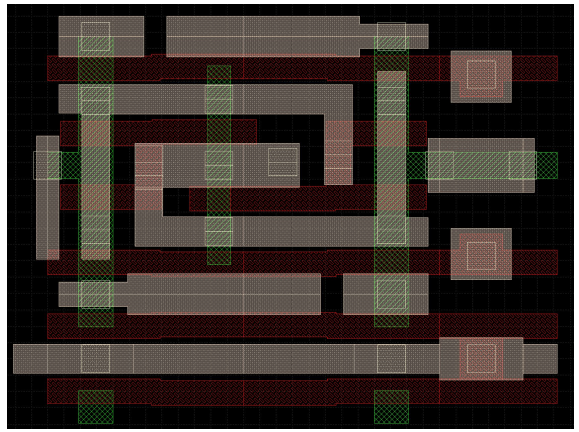
- An additional replica word line models the capacitance of the array's word line
- Dummy cells are not connected to the array bit lines (diffusion contacts are removed)
- Necessary for OPC and DRC



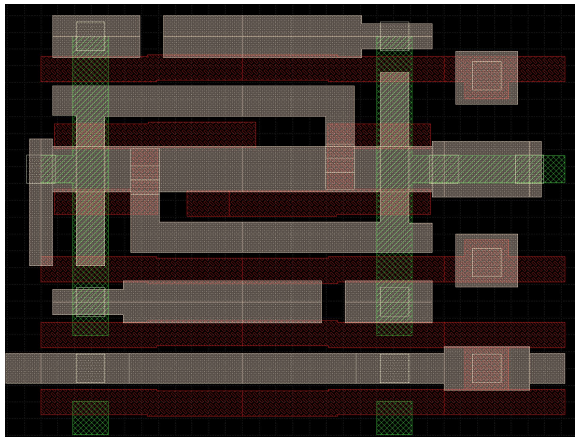
Single port array bitcell



Single port dummy bitcell



Dual port array bitcell



Dual port replica column bitcell

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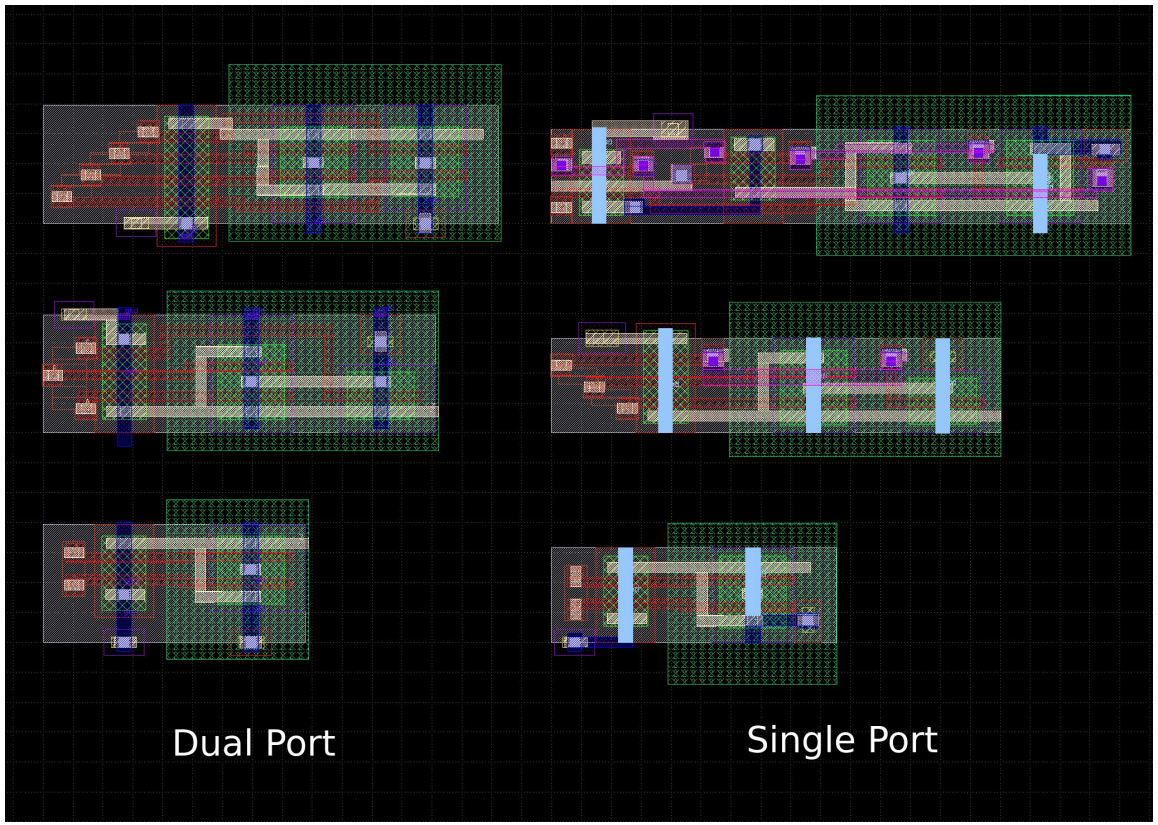
Word Line Decoder



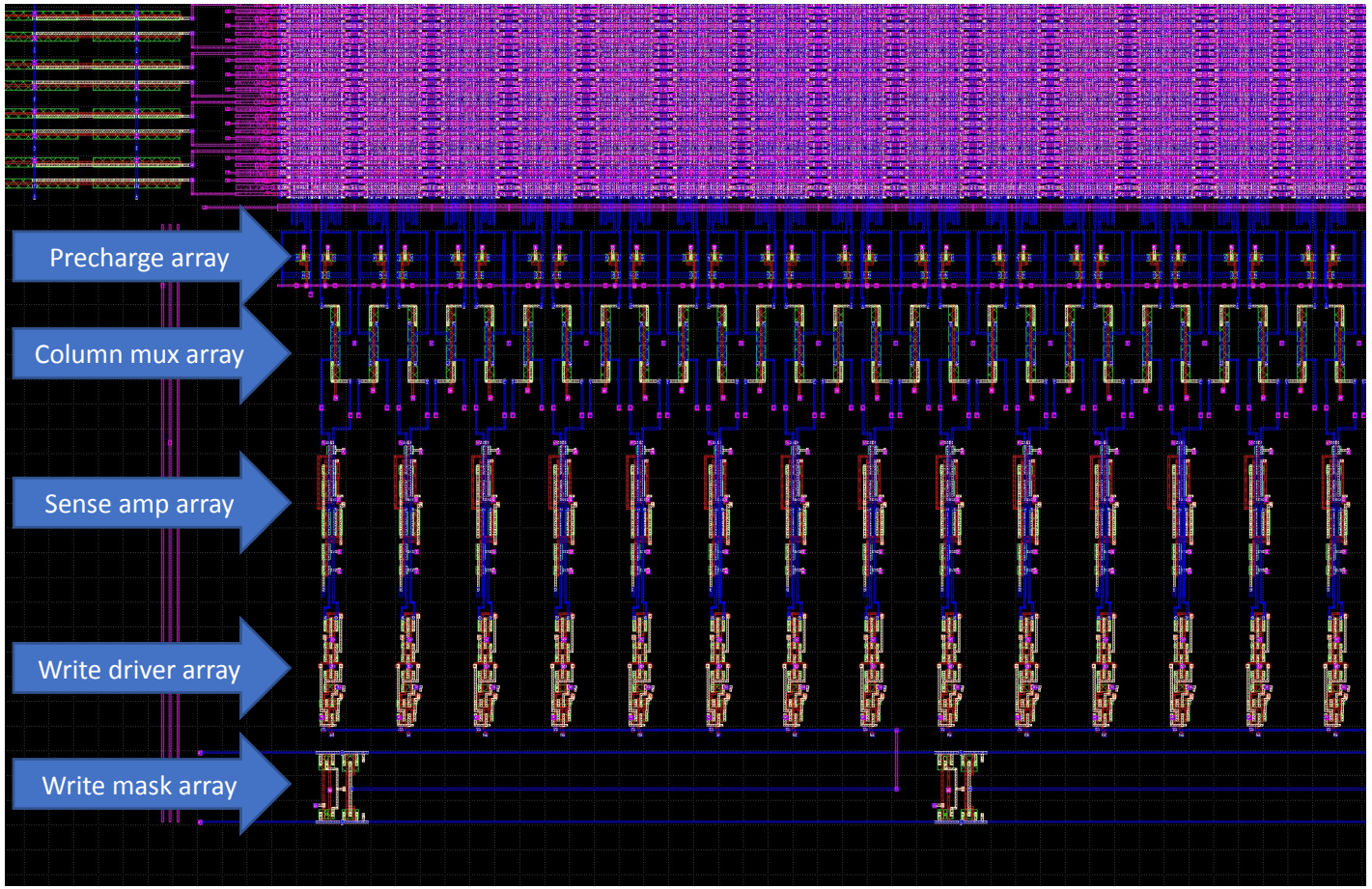
Custom NAND layouts. Top to bottom:
NAND4, NAND3, NAND2

- OpenRAM hierarchical decoders are generated from a NAND gate primitive
- OpenRAM can generated gate layouts have poor area
- Sky130nm required hand made NAND decoder cells to match pitch of bitcells
- Support max of 4096 rows
- ROM based decoder alternative is available but not integrated

OpenRAM

Data Port Logic

- Sense amplifier and write driver cells are reused from older OpenRAM supported technologies.
  - These match bitcell width to allow for optional no column muxing
- Other data circuitry such as the precharge array,column mux, and write mask are automatically generated



Port data for Sky130nm dual port macro

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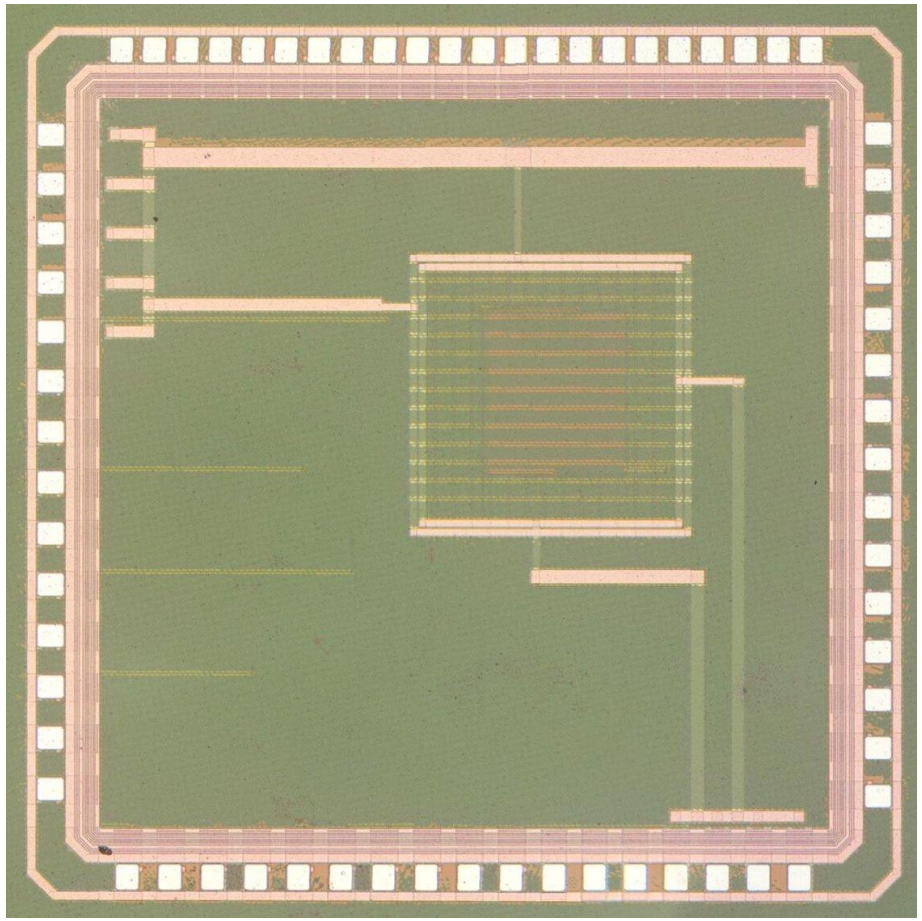
Tapeout – OR1

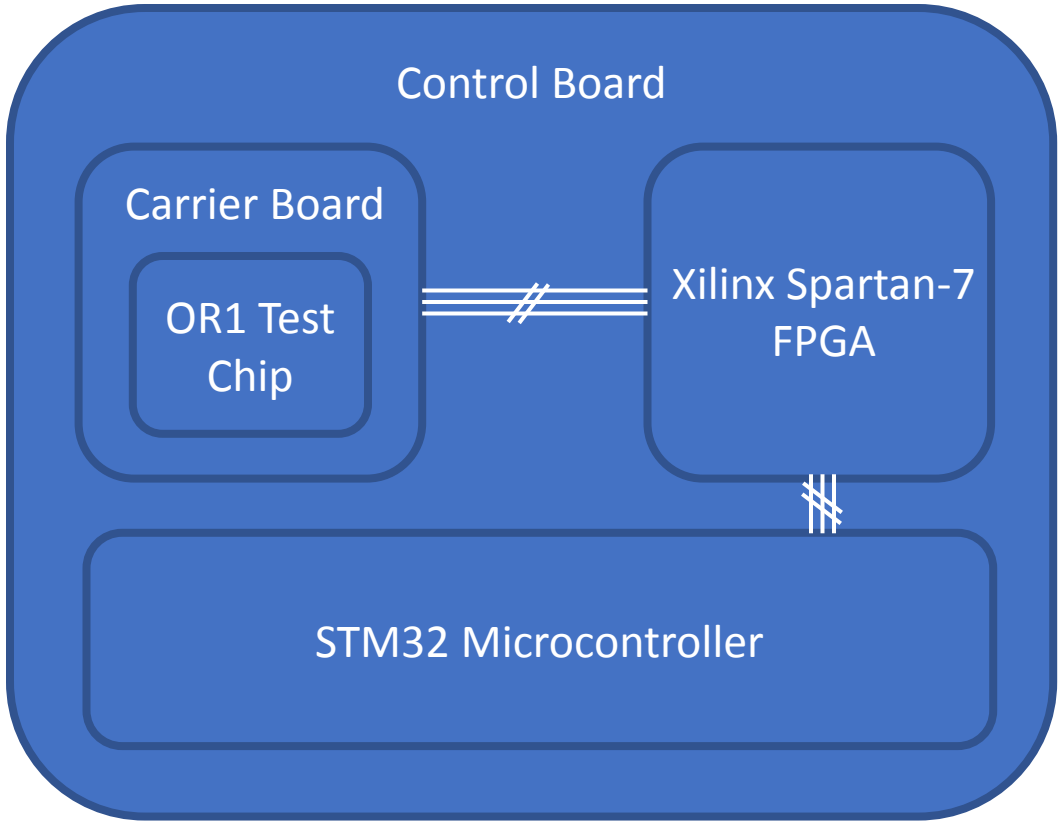
- Single 32bit 1kb 1RW1R SRAM macro
- SRAM control bonded out directly to I/O
  - Clock, chip select, write enable, and write mask signals
- Limited I/O so MSB and LSB of each byte (for each port) was bonded out
- Manual routing of core chip I/O
- Power grid over memory macro was manually routed to the supply rings



Tapeout – MPW2

- 5 single and 5 dual port SRAM macros
- Parallel on chip logic analyzer + GPIO for testing
- On-chip clock with off-chip backup
- Custom signal escape router for automatic routing of signals to macro perimeter
  - Enables compatibility with OpenLane Triton Route
- Power rings around memory and metal blocking LEF view
  - Enables compatibility with OpenLane power distribution network router

Test and Measurement – OR1

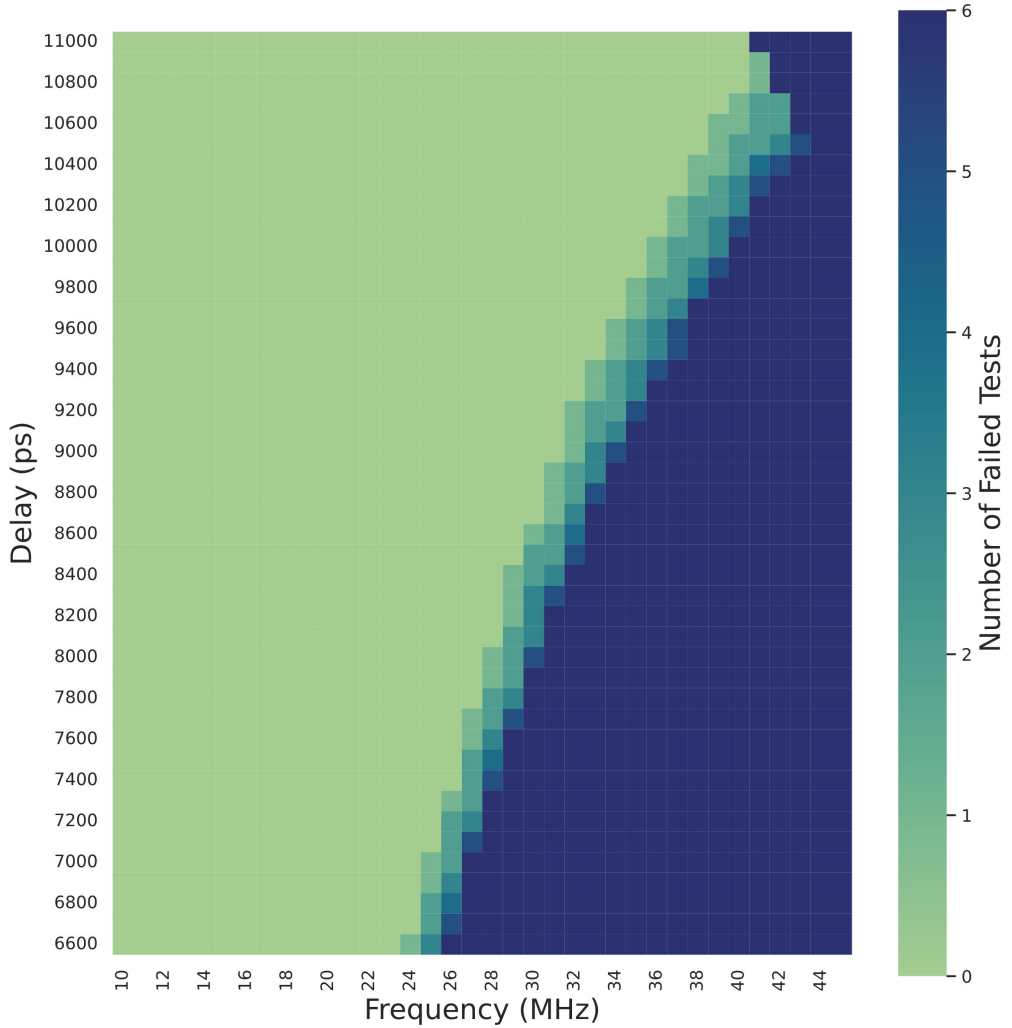


- All traces between FPGA to test chip are delay matched
- Read data registered in FPGA
  - FPGA PLL adjusted to output clock for propagation delays including that internal to the test chip
- No on-die temperature sensor
  - Temps measured through Peltier plate and the bottoms of PCB

OpenRAM

Test and Measurement – OR1

- Each point is tested for single and dual port operation at three different temperatures for 6 total tests
- 6.6ns min capture delay at 23Mhz
- 11ns min capture delay at 39Mhz



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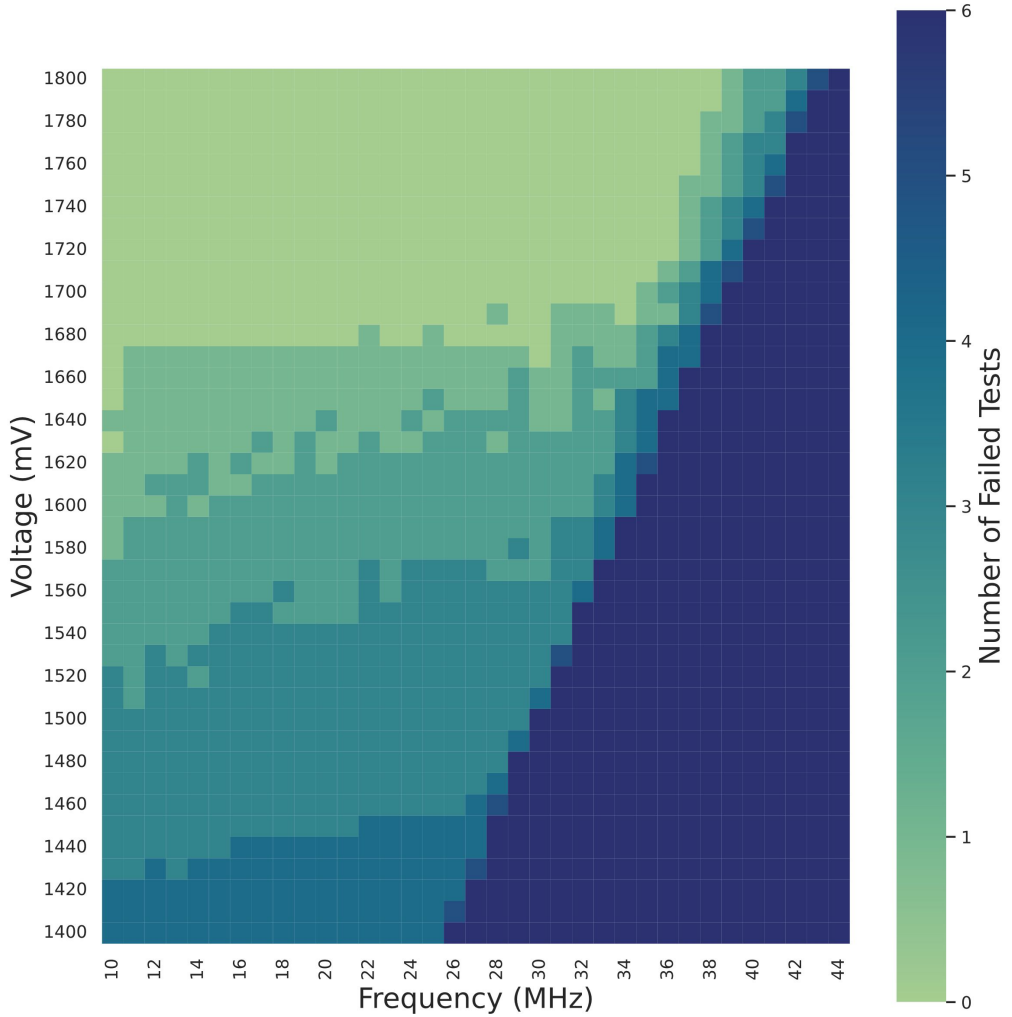
Test and Measurement – OR1

- No errors below 34Mhz at 1.7V
- For a single read port there are no errors below 25Mhz at 1.54V



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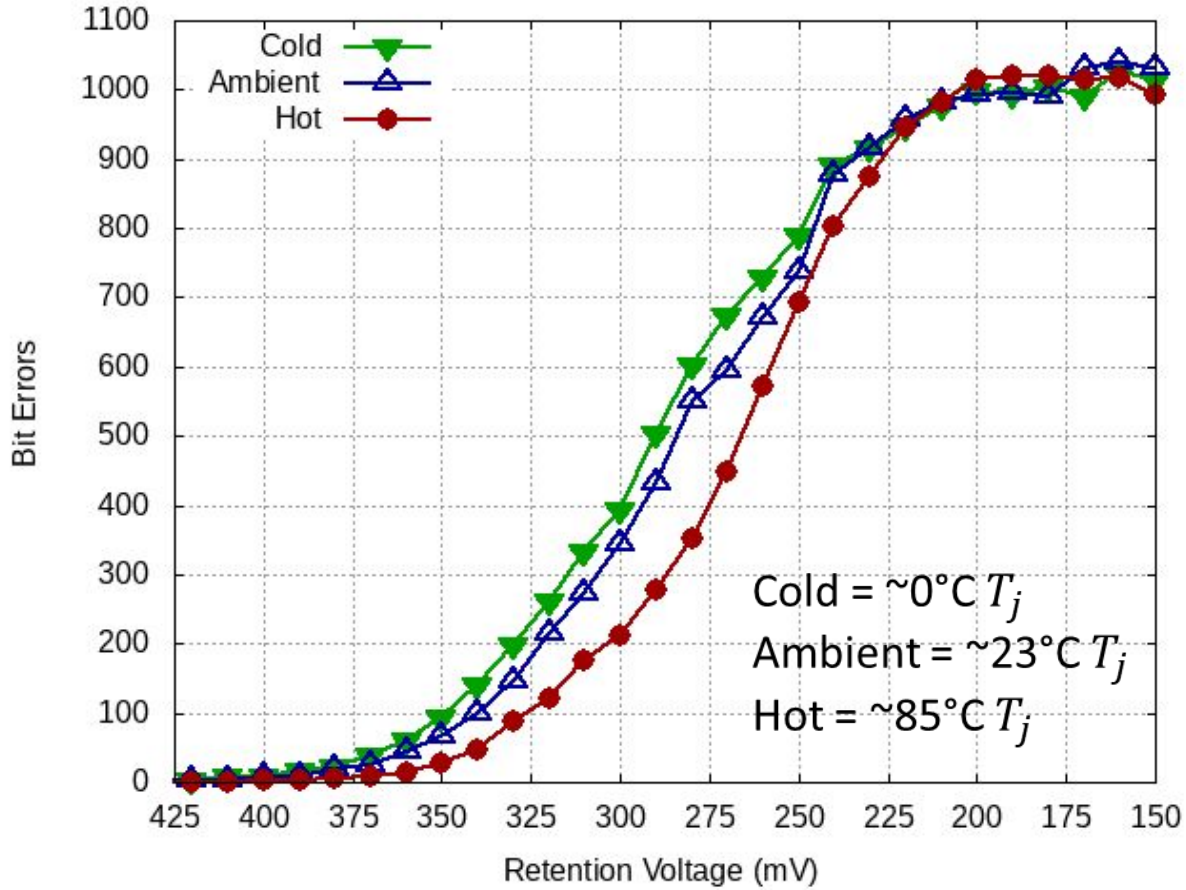
Test and Measurement – OR1

- First errors are observed at 440mV when cold and 410mV when hot



OpenRAM

Conclusions/Future WOrk

OpenROM just released (but not yet working in OpenLane)

Porting OpenRAM to GF180

ReRAM array structures