nextpnr & FABulous

customisable custom hardware

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nextpnr

- Development started May 2018
- Open source multi-architecture FPGA place & route aimed at real world FPGAs
- Support for a range of commercial FPGAs (Lattice, Intel, Gowin, experimentally Xilinx) as well as FABulous eFPGAs

nextpnr

- Viaduct framework enables rapid prototyping of custom architectures (e.g. eFPGAs)
- Support for the full range of customisable validity and packing rules – highly flexible CLBs, IP, …
- Viaduct scales up to ~25k LUT
- Full custom deduplicated arch up to 1M+ LUT (PnR algorithms maybe not quite)

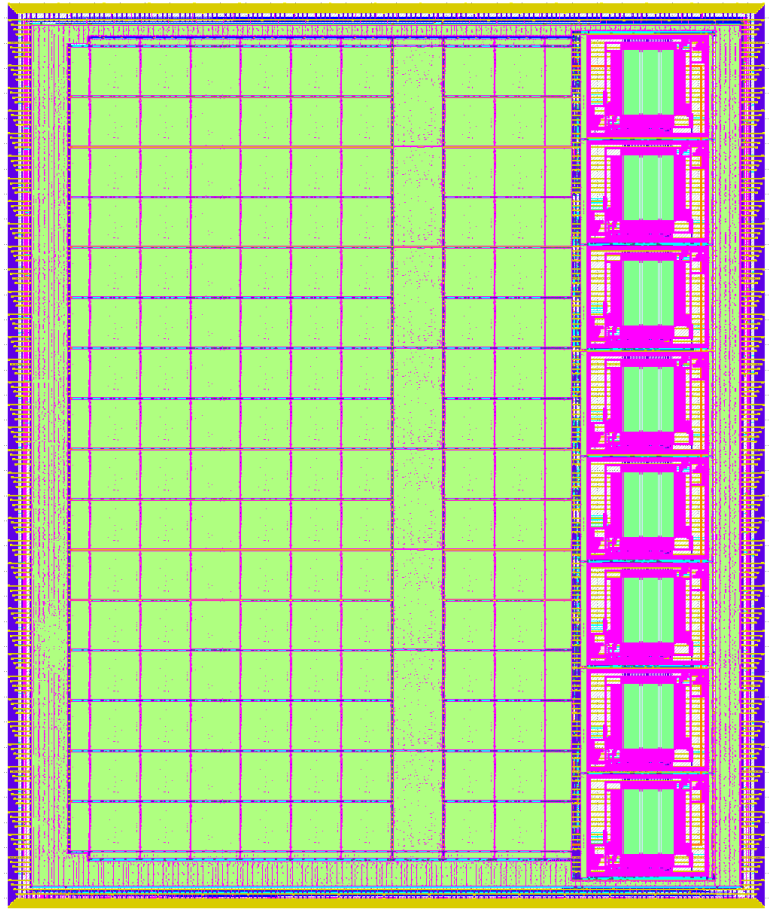
FABulous

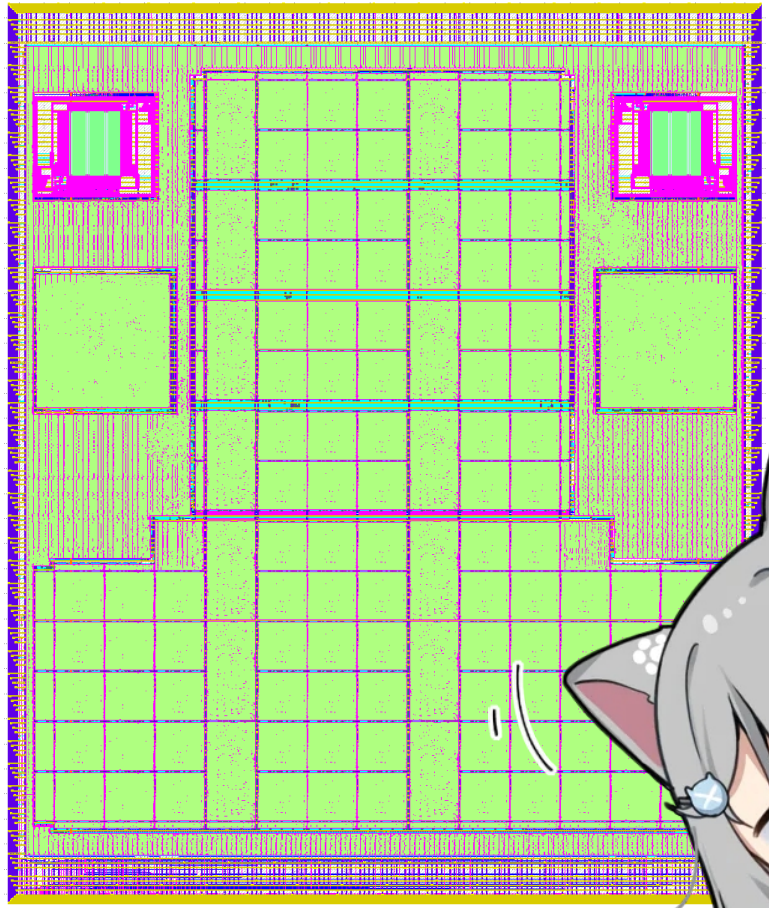
- eFPGA fabric generator from Manchester & Heidelberg Universities
- Support for custom blocks including DSP, BRAM, register files CPU interfaces, etc
- Tapeouts on open Google shuttle runs
- MPW2 samples back and working!

FABulous

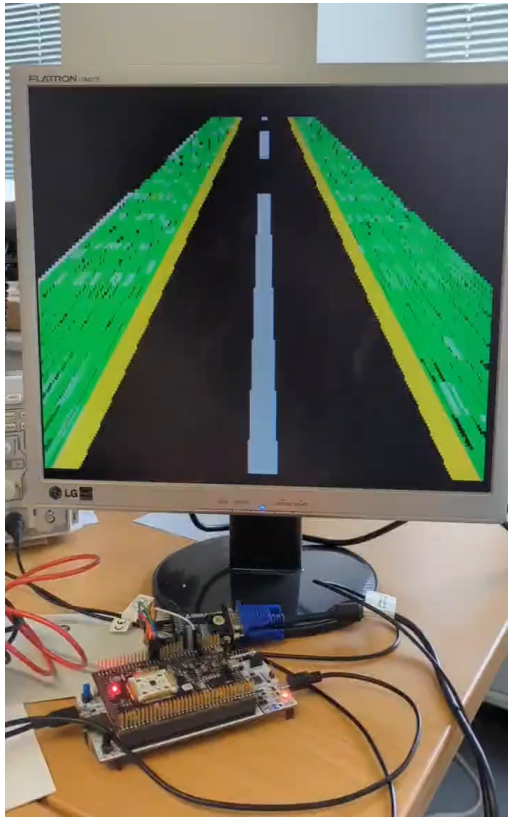
- Tile structure and routing graph described in simple text-based formats
- Generates Verilog or VHDL tiles and fabric; nextpnr data
- Latch-based configuration architecture, smaller and more robust than shift registers
- Partial reconfiguration

FABulous on MPW2





FABulous on MPW2



FABulous on MPW2

- LUTs, FFs, BRAM (OpenRAM), DSPs all working
- Some expected hold time problems due to clock routing structure
- Fixable in nextpnr (FPGAs make this easy) but we need a timing model...

The Future

- Improving nextpnr’s timing analysis to cross clock domains
- Adding a GUI for FABulous fabrics
- Electrostatic placer for nextpnr
- Rust bindings & partition-based router

Questions?

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Catgirl Credit: https://store.line.me/stickershop/product/12126860/en