

GHDL in the FOSS EDA ecosystem

Tristan Gingold

DATE - OSDA 2023/04/17

GHDL as a simulator

- Standard supported:
 - vhdl-93: full,
 - vhdl-08: mostly,
 - vhdl-2019: planned
- Compiled simulation (generation of CPU opcodes)
- Multiple backends: GCC, LLVM, mcode (internal)
- Fast translation
- But simulation speed varies...
- Better error messages
- Bugs can be fixed quickly

The simulation ecosystem

- Waveform generation for gtkWave
- VCD output (lowest common denominator)
- Limited debugging with gdb
- Coverage (with gcov)
 - Need something better
- Support of FOSS verification frameworks

Missing pieces

- Mixed languages simulation
 - FOSS Verilog/SystemVerilog exists
- IDE
 - Improve gtkWave to interface with simulators
 - Integration of waveform viewers within IDE
- Graphical design with blocks
 - Reuse schematic editors of PCB tools (like KiCad)
- Schematic viewer
- SystemVerilog: full support of UVM (wip)

GHDL for Editors

- `ghdl-ls` is a language server for VHDL
- Support for vs-code (but not in the market place)
- Navigation
 - jump to declaration / definition
 - Hover
- Reformatting
- Instantiation
- Error messages as you type

Why FOSS EDA tools ?

- For makers
 - Low money, but OK with free versions
- For FOSS activists
- For Industry: prototypes/CI
 - Could be faster than closed tools (no license check)
 - No license restriction (unlimited runs)

GHDL for synthesis

- Relatively recent feature (~2020)
- Wide support of vhdl features
 - Including at elaboration
- Non-optimized netlist generation (vhdl or verilog)
- Yosys plugin - easy integration
- Support of PSL (for formal proof)

Multi language support

- Incomplete support with Yosys
 - Can instantiate a design from any language
 - TODO: parameters/generics value
- Need mixed elaboration
- Cross module probing ?
- Cross language type definitions ?

My rant: vendor position ?

- Vendors are heavy users of FOSS
 - IDE: Eclipse
 - Compilers: LLVM, gcc
 - Languages: TCL, python...
 - Libraries: boost, json/xml parsers, http, tcp/ip stack,...
 - OS: Linux, FreeRTOS, uboot
- But poor openness:
 - No simulation models available
 - Encrypted or vendor specific libraries
 - Proprietary formats
 - Bitstream

Conclusion

- Long story of FOSS EDA:
 - Just think of Berkeley: Spice, TCL, Risc-V, espresso
- Still continuing
- Some tools are missing
 - In particular for beginners (eg: IDE)
- EDA vendors could be more open!