

# PACT: A SPICE-Based Parallel Compact Thermal Simulator for Fast Analysis

By Mohammadamin Hajikhodaverdian<sup>1</sup>, Zihao Yuan<sup>1</sup>, Sherief Reda<sup>2</sup> and Ayse K. Coskun<sup>1</sup>

<sup>1</sup>Boston University; <sup>2</sup>Brown University

Workshop on Open-Source Design Automation (OSDA) May 15, 2024



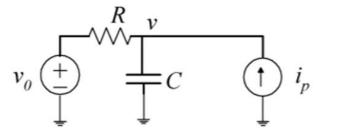


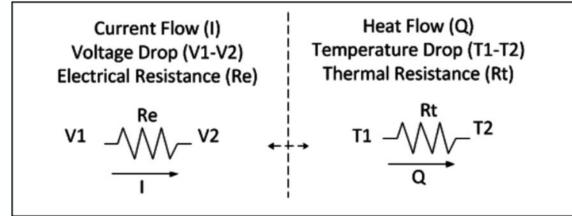
# Compact Thermal Modeling (CTM)

- Traditional thermal models
  - Finite element method (FEM)
  - Accurate but slow

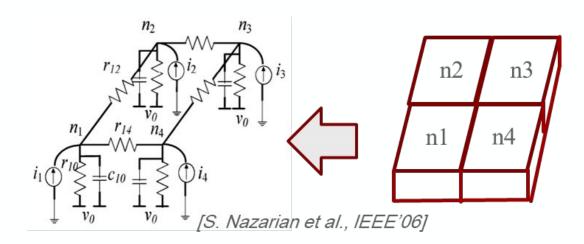
# • CTM

- Fast and accurate modeling methodology
- Duality between electric and thermal properties
- Lump resistor-capacitor (RC) circuit
- Chip can be modeled as a lump RC network





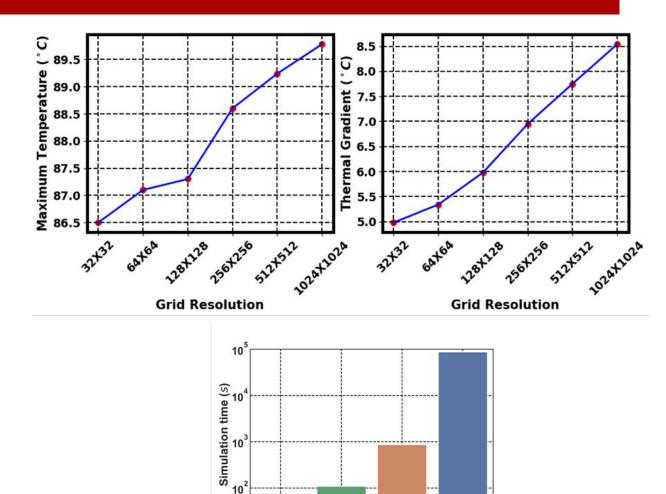




 $C\frac{dv}{dt} = \frac{v_0 - v}{R_E} + i_p$ 

# **Related Work**

- Challenges in existing compact thermal simulators
  - Target architecture-level thermal simulations
    - HotSpot [K. Skadron et al., ISCA'10]
    - 3D-ICE [A. Sridhar et al., ICCAD'10]
  - Cannot tackle large and complex problems
    - Standard-cell designs
    - Monolithic 3D simulations
  - Hard to extend emerging integration and cooling technologies
    - New models for cooling methods frequently roll out customized software package



[Z. Yuan et al., TCAD'21]

Chip thickness (µm)

1.0

0.1

10.0

100.0

## Contributions of PACT

## PACT: Parallel Compact Thermal Simulator

- Fast and accurate
- Standard-cell level to architecture-level
- High extensibility
- Interface to OpenROAD [T.Ajayi et al., DAC'19]
- Open-sourced simulator: <u>https://github.com/peaclab</u>
- VisualPACT

Accuracy vs. other thermal simulators:

- 3.28% vs. COMSOL
- < 0.5% vs. HotSpot
- 1.12<sup>°C</sup> vs. 3D-ICE

#### Speed vs. HotSpot:

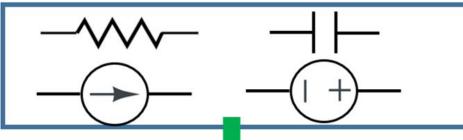
- Steady-state: I.8X
- Transient: 186X

## **PACT** Simulation Flow

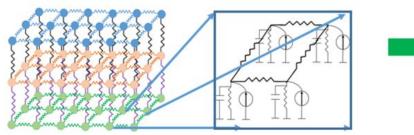
#### **User inputs**

- Chip stack descriptions
- # of grids and heat sink type
- Material properties and cooling method

## Calculate netlist components



### Thermal netlist generator



## SPICE Engine Outputs CSV Parallel configuration (OpenMPI) # of Node, # of Cores ٠ Parallel option (e.g., -bind-to none) ٠ Job mapping option (e.g., -cpu-set) Simulation type and solver selection Steady-state (e.g., KLU, KSparse) Transient (e.g., Backward Euler, Trapezoidal) ٠ Options (e.g., time period, step size) ٠

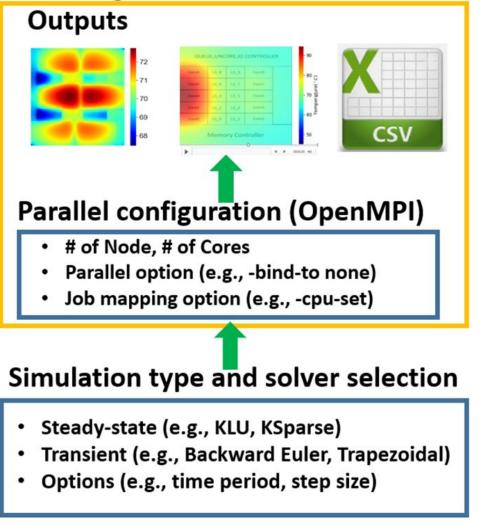
## PACT Simulation Flow

#### **User inputs**

- Chip stack descriptions
- # of grids and heat sink type
- Material properties and cooling method

| Symbol        | Component name                       | Equivalent terminology in PACT  |  |  |  |  |  |  |  |
|---------------|--------------------------------------|---|--|--|--|--|--|--|--|
|               | Resistor                             | Thermal Resistor  |  |  |  |  |  |  |  |
|               | Capacitor                            | Thermal Capacitor   |  |  |  |  |  |  |  |
|               | Current source                       | Heat flow (power)<br>Liquid convection in<br>microchannel grid                    |  |  |  |  |  |  |  |
| $\rightarrow$ | Voltage-controlled<br>current source |   |  |  |  |  |  |  |  |
| +             | Voltage source                       | Assign initial temperature and<br>ambient temperature                             |  |  |  |  |  |  |  |
|               | PWL current source                   | Enable transient thermal<br>simulation with step response<br>or real power traces |  |  |  |  |  |  |  |

#### **SPICE Engine**



# Extensibility of PACT

#### Liquid cooling input parameters

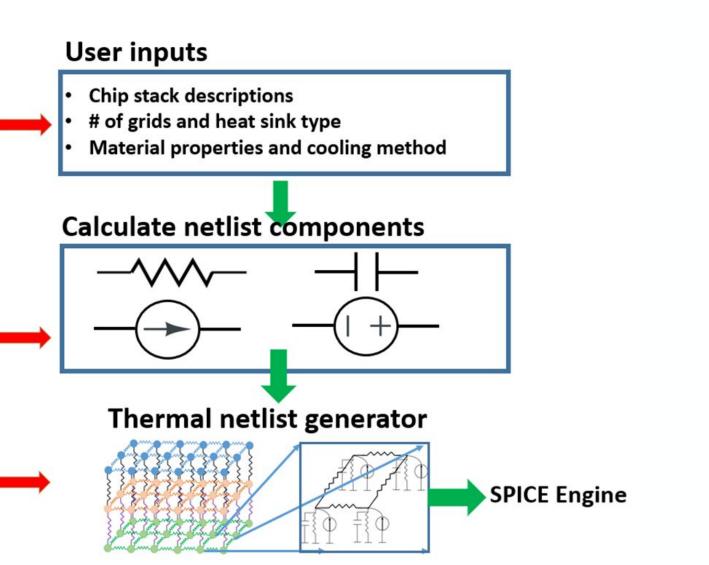
[Liq] Thermal resistivity ((m-k)/w) = 1.647 Specific heat capacity (j/m^3k) = 4.181e6 inlet\_temperature (Celsius) = 27 fluid\_density (kg/m3) = 998 dynamic\_viscosity (pa.s) = 8.89e-4 coolant\_velocity (m/s) = 0.5 num\_of\_channels = 2

#### Liquid.py



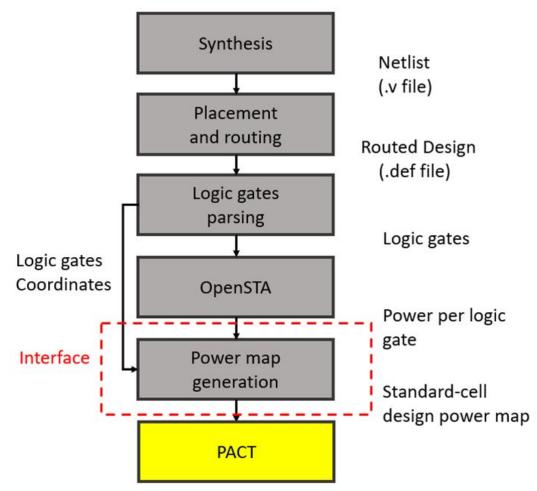
#### Liquid grid cell information

[Liq] library\_name = Liquid library = Liquid.py virtual\_node = center\_center



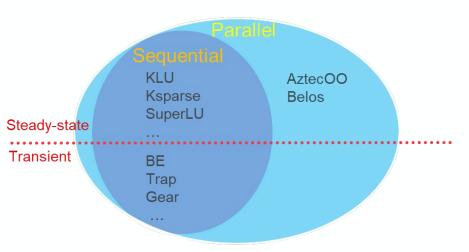
## **OpenROAD** Interface and PACT Solvers

### **OpenROAD** Interface



### **PACT** Solvers

- Direct solver vs. Iterative solver
- Numerical instability issue with Forward Euler method (Monolithic 3D transient simulation)
- Simulation speed and accuracy tradeoff

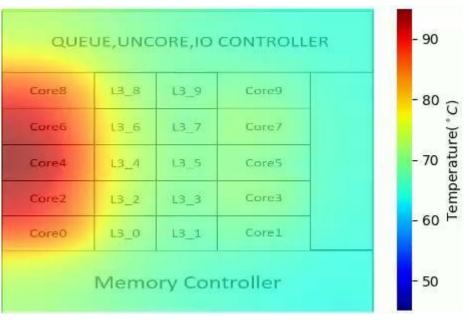


# VisualPACT

## • VisualPACT

- Generating thermal videos for transient thermal simulations
- Visualizing transient thermal behaviors of architectural simulations

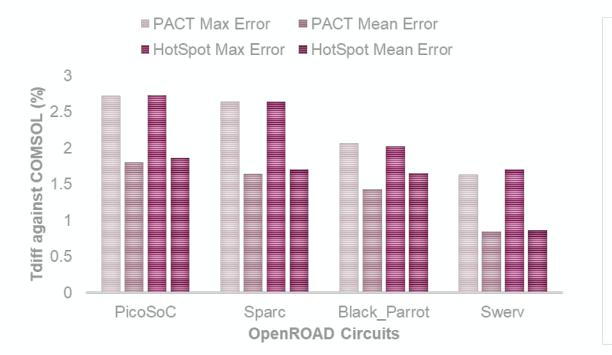
#### VisualPACT (Intel i7 6950X)

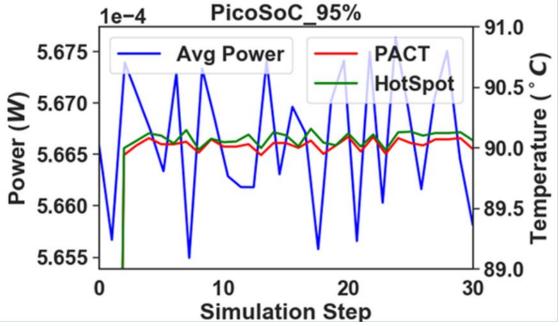


### Validation with OpenROAD Benchmarks

#### Steady-State vs. HotSpot

Transient vs. HotSpot

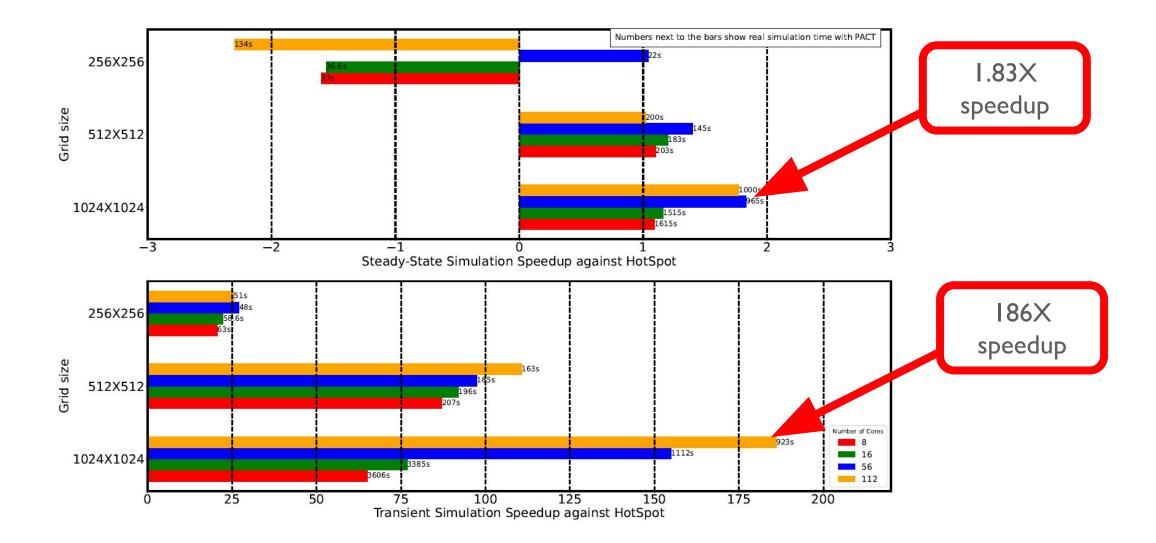




PACT vs. COMSOL (Max Steady-State Diff: 2.77%)

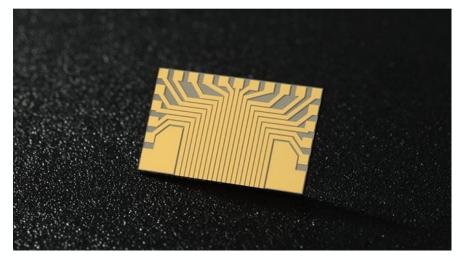
PACT vs. COMSOL (Max Transient Diff: 3.28%)

# PACT Speed Analysis against HotSpot



# PACT Case Study: Lab-Grown Diamond Heat Spreaders

- High thermal conductance compared to the copper heat spreaders
- Can be bonded directly to the processor's layer w/o thermal interface
- Diamond heat spreaders vs. copper heat spreaders



## PACT Case Study: Lab-Grown Diamond Heat Spreaders

Chip stack #1 (Copper)

Chip stack #3 (Diamond)

| QUEUE, UNCORE, IO CONTROLLER |      |      | QUEUE, UNCORE, ID CONTROLLER |  |       |      | ER   | - 90  |  |                            |
|------------------------------|------|------|------------------------------|--|-------|------|------|-------|--|----------------------------|
| Core8                        | L3_8 | L3_9 | Core9                        |  | Core8 | L3_8 | L3_9 | Core9 |  | - 80 <sub>C</sub>          |
| Core6                        | L3_6 | L3_7 | Core7                        |  | Coreő | L3_6 | L3_7 | Core7 |  |                            |
| Core4                        | L3_4 | 13_5 | Core5                        |  | Core4 | L3_4 | 13_5 | Core5 |  | •<br>Temperature<br>- 00 - |
| Core2                        | L3_2 | L3_3 | Core3                        |  | Core2 | L3_2 | L3_3 | Core3 |  | empe                       |
| Core0                        | L3_0 | L3_1 | Corel                        |  | Core0 | L3_0 | L3_1 | Core1 |  | - 60 🖵                     |
| Memory Controller            |      |      | Memory Controller            |  |       |      |      | - 50  |  |                            |
|                              |      |      |                              |  |       |      |      |       |  |                            |
|                              |      |      |                              |  |       |      |      |       |  |                            |
|                              |      |      |                              |  |       |      |      |       |  |                            |

Hot Spot temperature reduction>20°C

- Enable easy adoption without having to install dependencies (i.e., Xyce SPICE simulator)
- Use Docker to build a new image



#### BOSTON UNIVERSITY



# • PACT

- Fast and accurate parallel thermal simulator
- Architecture level & standard-cell level
- High extensibility for emerging cooling methods
- Various numerical solvers
- OpenROAD interface
- VisualPACT

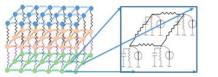
#### User inputs

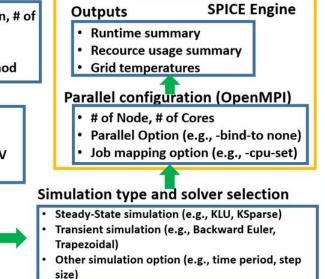
- Chip stack descriptions (e.g., floorplan, # of layers, power traces)
- # of grids and heat sink type
- Material properties and cooling method

#### Calculate netlist components

- Calculate thermal R, C, and I
- Calculate package thermal R and C
- Calculate thermal R, C, and I for TSV and cooling methods

#### Thermal netlist generator





# CONCLUDING REMARKS



More info at https://github.com/peaclab/PACT Please send feedback to aminhaji@bu.edu