Coriolis – A FOSS RTL to GDSII Toolchain

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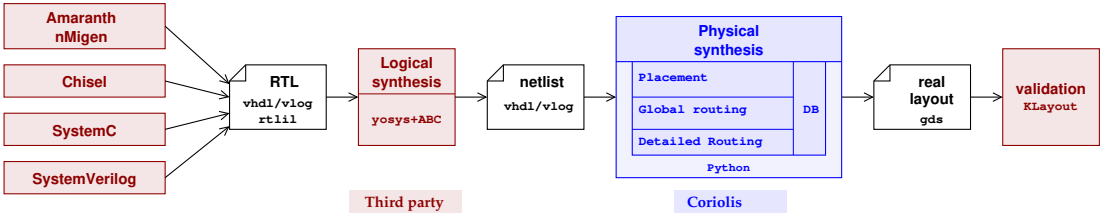
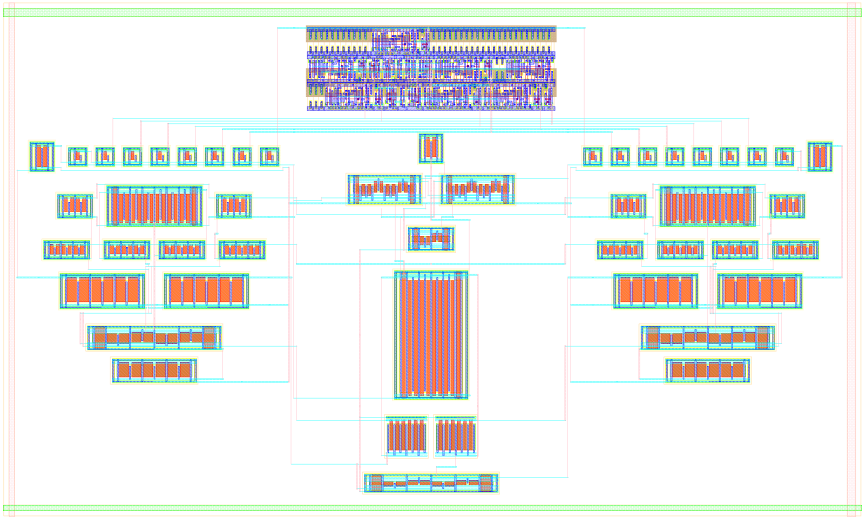
A General Overview

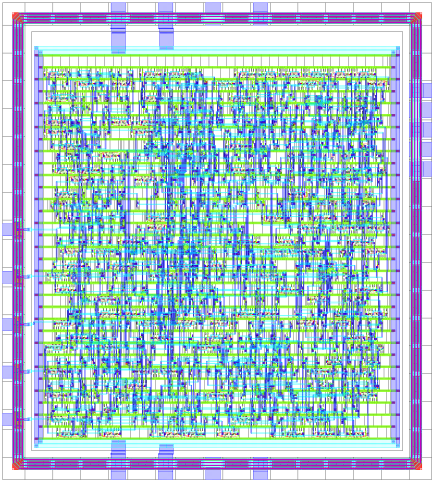


- The Coriolis EDA toolchain.
- Current capabilities.
- Future features & strategy.
- The challenges of building a toolchain.

Mixed Designs

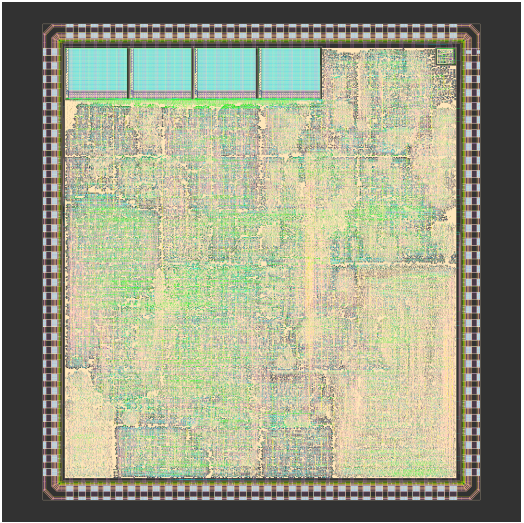


Thermometer test chip



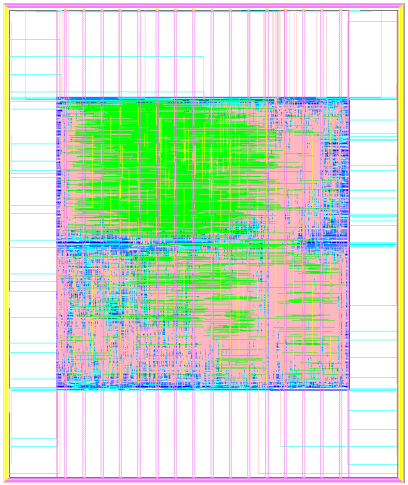
- Designed by ChipFlow, `https://chipflow.io/`
- PragmatIC Flexible IC 0.8µm, `https://pragmaticsemi.com`
- 760 standard cells.

The LibreSOC chip



- https://libre-soc.org/.
- TSMC 180nm.
- 1.3 Mt, standard cells: 500 Kt, SRAM: 800 Kt.
- 120K gates (SRAM excluded).
- 5.1 $\times$ 5.5 mm ($28mm^2$).

The Minerva RISC-V chip



- Done by ChipFlow, `https://chipflow.io/`
- Contains a Minerva RISC-V RV32IM, `https://github.com/minerva-cpu/minerva`
- SkyWater 130nm (Google MPW4).
- Use the E-fabless Caravel Harness `https://github.com/efabless/caravel`.
- 220K transistors, 57K gates.